

Application No.: 09/517,314

Docket No.: M4065.0223/P223

REMARKS

Claims 1, 3-4, 9-10, 18, and 22-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fig. 11 of Chiang in view of Fig. 9 of Chiang. This rejection is respectfully traversed.

The Office Action contends that Fig. 11 discloses Applicant's invention except for a first and second conductor layer. To rectify this deficiency, the Office Action asserts that Fig. 9 of Chiang teaches a first and second conductor layer. However, it is illogical to combine Chiang's Fig. 9 with Fig. 11.

Claim 1 recites a semiconductor device comprising, "an insulator layer, a conductive plug . . . formed of a single conductive material, an etch-stop layer . . . a non-conductive layer having an etched via . . . wider in diameter than said conductive plug, and a conductive connector . . . including a first conductive layer . . . and a second conductive layer."

Chiang discloses that "FIGS. 10 and 11 illustrate an alternate embodiment of the present invention." (Col. 11, lines 12-13) (emphasis added). Fig. 11 is an alternative embodiment which only teaches and suggests a single conductor layer provided with a single conductive plug and not "a first conductive layer . . . and a second conductive layer," as recited in claim 1. Fig. 11 teaches using aluminum as the interconnect material with the associated structure (Col. 11, lines 19-31), whereas FIG. 9 is directed to providing a copper interconnect material (61) that is surrounded by a diffusion barrier layer (60) (FIG. 9). There is no motivation to combine the two figures since they are directed to providing alternate embodiments employing different interconnect materials. ② ←

Further, the combination of Chiang's FIG. 11 with FIG. 9, results in a larger semiconductor device which would "consume considerable amount of area on the chip, thereby limiting scaling." (Col. 10, lines 29-30). In particular, the line width of the aluminum interconnect taught in Chiang's FIG. 11 is "greater than the line width of the

Application No.: 09/517,314

Docket No.: M4065.0223/P223

copper interconnects of FIG. 9.” (Col. 11, lines 43-45) (emphasis added). “[T]he presence of the widened region on each interconnect line causes adjacent interconnects to be spaced further apart than if no widened region were present.” (Col. 10, lines 33-35). As a result, there is no motivation to combine FIG. 11 and FIG. 9 since FIG. 11 would inhibit scaling of the chip since it would possess a larger line width than the FIG. 9 embodiment. (D) ←

In fact, one of the benefits of Chiang’s invention is that “the interconnects of the present invention can be the same width at the contact region.” (Col. 10, lines 36-37). There is no motivation to combine Chiang’s FIG. 9 with FIG. 11 since a wider interconnect would result. Applicants respectfully submit that the combination of the Fig. 9 and 11 embodiments is an impermissible hindsight reconstruction of the invention. ←

Claims 3-4, and 9-10 depend from and contain all of the limitations of claim 1. Accordingly, claims 3-4 and 9-10 are allowable for at least the reasons set forth above for allowance of claim 1.

Claims 5-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang in view of Wang. Claims 5-6 depend from and contain all of the limitations of claim 1. Accordingly, claims 5-6 are allowable for at least the reasons given above for allowance of claim 1.

Moreover, Chiang does not teach or suggest that the “etch-stop layer comprises silicon nitride and silicon carbide,” as recited in claim 6 (emphasis added). This is an additional reason for the allowance of claim 6.

Claims 7-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang in view of Hong. Claims 7-8 depend from and contain all of the limitations of claim 1. Accordingly, claims 7-8 are allowable for at least the reasons given above for allowance of claim 1.

Application No.: 09/517,314

Docket No.: M4065.0223/P223

Claims 11, 15-17, 25, 27, 30-32, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang's FIG. 11 in view of FIG. 9 and further in view of Matsuura. Reconsideration is respectfully requested.

As discussed above, Chiang does not teach or suggest a structure with two conductive layers over a plug formed of a single conductive element. In particular, there is no motivation to combine Chiang's FIG. 11 with FIG. 9 since the embodiment taught in FIG. 11 is an alternate embodiment that completely teaches a different line width, e.g., a much wider line width than FIG. 9's embodiment.

Chiang does not teach or suggest, "a conductive plug formed of a single conductive material . . . an etch-stop layer . . . an intermediate non-conductive layer provided over said etch stop layer and having at least a first and second etched via over said plug, said first etched via being wider in diameter than said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via and a first conductive layer . . . and a second conductive layer," as recited in claim 11, nor a "a conductive plug formed of a single conductive material . . . an etch-stop layer . . . an intermediate non-conductive layer provided over said etch stop layer and having at least a first and second etched via over said plug, said first etched via being wider in diameter than said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via and . . . a conductive connector comprising a first conductive layer. . . and a second conductive layer," as recited in claim 25. ←

Moreover, the combination of Chiang and Matsuura is improper. There is no ← motivation to have a first and second etched via over a single conductive plug. Chiang teaches that "more than one level of interconnects as shown in FIG. 9," can be formed (Col. 10, lines 50-52). Chiang does not teach or suggest "an intermediate non-conductive layer provided over said etch stop layer and having at least a first and second etched via over said plug, said first etched via being wider in diameter than said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via," as

Application No.: 09/517,314

Docket No.: M4065.0223/P223

recited in claims 11 and 25. Further, the presence of a first and second etched via larger than the first via would increase the line width of the interconnect.

As discussed above, one of the benefits of Chiang's invention is that "the interconnects of the present invention can be the same width at the contact region." (Col. 10, lines 36-37). There is no motivation to form an interconnect channel that is wider when Chiang teaches that a benefit of the invention is increased scaling ability. That is, the combination proposed is directly contrary to the result sought by Chiang.

Claims 15-17 depends from and contains all of the limitations of claim 11, and claims 27, 30-32, and 39 depend from and contain all of the limitations of claim 25. Accordingly, claims 15-17 are allowable for at least the reasons set forth above for allowance of claim 11, and claims 27, 30-32, and 39 are allowable for at least the reasons set forth above for allowance of claim 25.

Claims 13-14 and 28-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang in view of Matsuura. Claims 13-14 depend from and contain all of the limitations of claim 11. Similarly, claims 28-29 depend from and contain all of the limitations of claim 25. Accordingly, claims 13-14 and claims 28-29 are allowable for at least the reasons given above for allowance of claims 11 and 25 provided above.

BEST AVAILABLE COPY

Application No.: 09/517,314

Docket No.: M4065.0223/P223

There are several important features of claims 1, 3-11, 13-17, 25, 27-32, and 39 that are not taught anywhere in the cited prior art. Accordingly, the rejection of claims 1, 3-11, 13-17, 25, 27-32, and 39 should be withdrawn. Allowance of the application with claims 1, 3-11, 25, 27-32, and 39 is respectfully solicited.

Dated: June 17, 2003

Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

DICKSTEIN SHAPIRO MORIN &  
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorney for Applicants